## ABSTRACT

A unified tag subsystem for a multilevel cache memory system. The unified tag subsystem receives a cache line address including a tag index portion, a high order part and an optional cache line extension field. The tag index portion indexes a tag memory which has way-specific address tags, and lower level flags. A comparator compares the high order part with each way-specific address tag to detect a match. Lower level hit logic determines a hit when comparator detects a match and the lower level flag indicates a valid lower level cache entry; and an upper level hit logic determines a higher level cache hit when the comparator detects a match and the upper level valid is set. In particular embodiments, lower level flag indicates a way of storage where associated data may be found in lower level cache data memory.